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4. TITLE AND SUBTITLE

High-Performance Integrated Circuit Evaluation System for a Gallium Arsenide Microsupercomputer

5. FUNDING NUMBERS

DAAL03-91-G-0223

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

University of Michigan
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8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

U. S. Army Research Office
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ARO 29305.1-EL

11. SUPPLEMENTARY NOTES

The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.

12a. DISTRIBUTION / AVAILABILITY STATEMENT

Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

This grant was used to extend an HP82000 High-Speed Digital IC Tester by adding 40 200-MHz channels and 16 400-MHz channels, along with associated power supplies, system racking, and accessories. The current configuration has a total of 176 1/0 channels.

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ARO 29305.1-EL

Final Report

1. ARO Proposal Number: 29305-EL
2. Period Covered by Report: 1 July 1991 — 31 December 1991
3. Title of Proposal: High-Performance Integrated Circuit Evaluation System for a Gallium Arsenide Microsupercomputer
4. Contract or Grant Number: DAAL03-91-G-0223
5. Name of Institution: University of Michigan
6. Author of Report: Richard B. Brown
7. List of Manuscripts:

   Since this is an equipment grant, it cannot be properly credited with supporting publications. Many of the papers published under ARO Proposal Number 28325-EL, however, are made possible because of the IC tester funded under this grant. (See progress report for 28325-EL.) Availability of the tester will also enable research and publications in a number of other DOD-funded projects.

8. Scientific Personnel Supported and Degrees Awarded:

   No personnel were supported; no degrees were awarded. The person responsible for the equipment is:

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on sabbatical at Cascade Design Automation, 3650 131 Ave. S.E., Bellevue, WA 98006)

9. Report of Inventions: None

Brief Outline of Research Findings

This grant of $149,202 from the U.S. Army Research Office was used to extend an HP82000 High-Speed Digital IC Tester by adding 40 200-MHz channels and 16 400-MHz channels, along with associated power supplies, system racking, and accessories. The current configuration has a total of 176 I/O channels.

Testers of this type, which allow researchers to work with the high-performance VLSI circuits of the next generation, are expensive. The funding of this equipment is a fine example of cooperation between government agencies, a university, and an equipment vendor to extend this capability to university researchers. The ARO grant complemented University of Michigan cost sharing on a DARPA contract of $85,000, University of Michigan College of Engineering support of $153,664, and a vendor discount of $205,518.

The tester is fully installed and operational in the Solid-State Testing Lab, room 1434 EECS, which also houses a variety of test equipment which can be used in conjunction with the IC Evaluation System. Access to this room is controlled by a magnetic-card system which also controls and monitors use of the solid-state clean room. Card-access both protects the equipment and makes it available 24 hours a day. The heat load of the tester requires additional air conditioning capacity in the room, which is being installed with support from the EECS department and research funds.

A number of integrated circuits have been tested now, the most interesting of which is the first GaAs CPU designed in our DARPA project as a test vehicle for our design automation tools. This is a reduced-function version of the MIPS architecture; the circuit consists of 60,500 transistors, measures 12.175 × 7.941 mm, dissipates 11 watts, and executes 28 instructions. This first CPU was designed by five students in five months, including writing the cell generators for the GaAs circuit compiler. It has only one design error (source-follower buffers driven by lines that also drive DCFL gates), found just after the design was submitted to MOSIS for fabrication. Correct operation of the CPU has been verified on the HP82000 at 100 MHz clock frequency. Higher-speed testing is under way. The next CPU in this project, scheduled for design completion in March 1992, will fully utilize the speed capability of the tester